

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,170,361 B1
APPLICATION NO. : 09/548942
DATED : January 30, 2007
INVENTOR(S) : Farnworth

Page 1 of 7

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Delete Title page illustrating a figure(s), and substitute therefor, new Title page illustrating a figure(s). (attached)

In item (56), "References Cited,"

U.S. PATENT DOCUMENTS,
2nd column, 10th entry:

Delete "6,262,660 B1 * 7/2001 Segale et al.
...257/728"
and insert in its place:
--6,232,660 B1 * 5/2001 Kakimoto et al.
.....257/728--

In the drawings:

In FIG. 1,	replace the informal drawing of FIG. 1 with the formal drawing of FIG. 1
In FIG. 2,	replace the informal drawing of FIG. 2 with the formal drawing of FIG. 2
In FIG. 3,	replace the informal drawing of FIG. 3 with the formal drawing of FIG. 3
In FIG. 4,	replace the informal drawing of FIG. 4 with the formal drawing of FIG. 4
In FIG. 5,	replace the informal drawing of FIG. 5 with the formal drawing of FIG 5
In FIG. 11,	replace the drawing of FIG. 11 with FIG. 11 amended on April 4, 2006, by inserting reference numerals --28-- and --29-- (two occurrences each)
In FIG. 12,	replace the informal drawing of FIG. 12 with the formal drawing of FIG. 12
In FIG. 13,	replace the informal drawing of FIG. 13 with the formal drawing of FIG.13
In FIG. 14,	replace the informal drawing of FIG. 14 with the formal drawing of FIG.14
In FIG. 15,	replace the informal drawing of FIG. 15 with the formal drawing of FIG.15

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings (cont'd):

Please replace FIG. 1 with the following replacement figure:

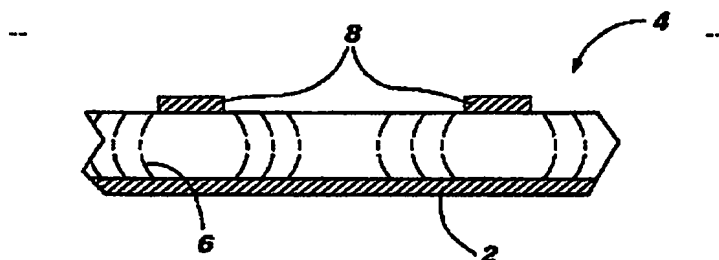


Fig. 1
(PRIOR ART)

Please replace FIG. 2 with the following replacement figure:

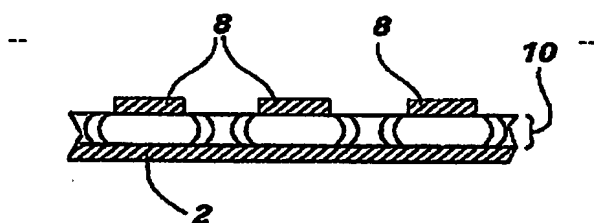


Fig. 2
(PRIOR ART)

Please replace FIG. 3 with the following replacement figure:

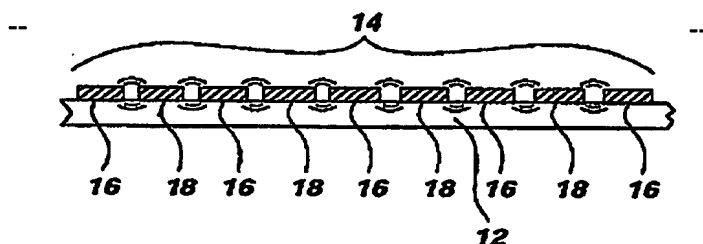


Fig. 3

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings (cont'd):

Please replace FIG. 4 with the following replacement figure:

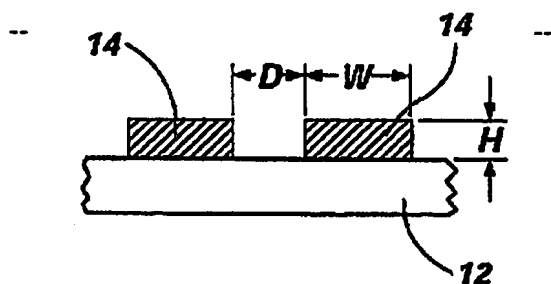


Fig. 4

Please replace FIG. 5 with the following replacement figure:

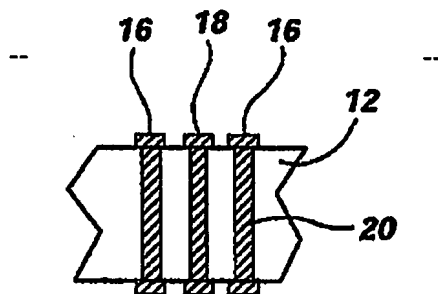


Fig. 5

Please replace FIG. 11 with the following replacement figure:

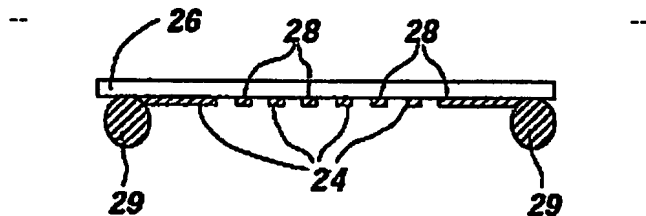


Fig. 11

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings (cont'd):

Please replace FIG. 12 with the following replacement figure:

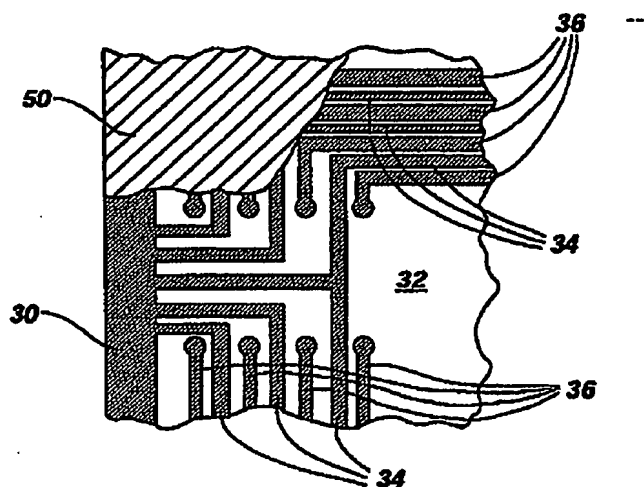


Fig. 12

Please replace FIG. 13 with the following replacement figure:

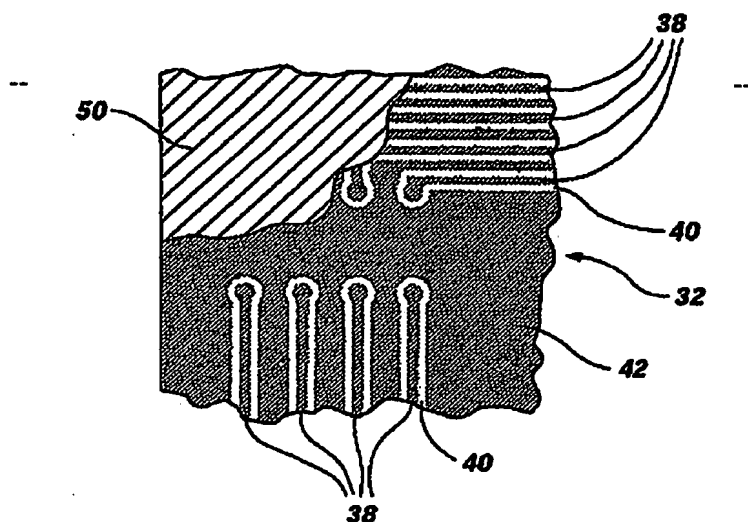


Fig. 13

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings (cont'd):

Please replace FIG. 14 with the following replacement figure:

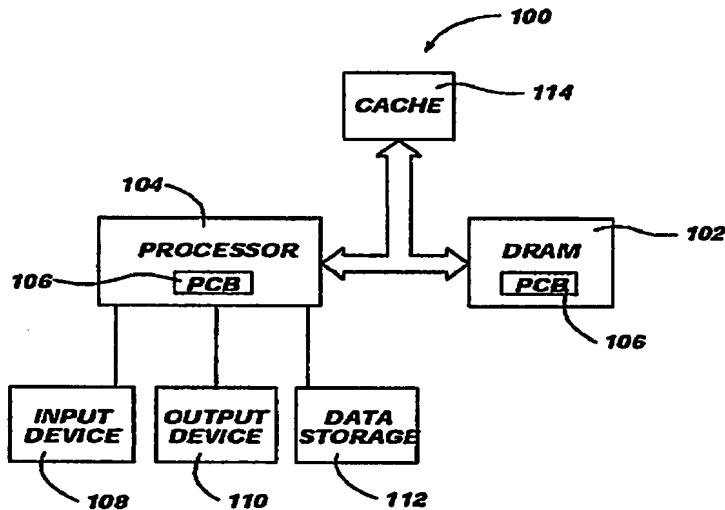


Fig. 14

Please replace FIG. 15 with the following replacement figure:

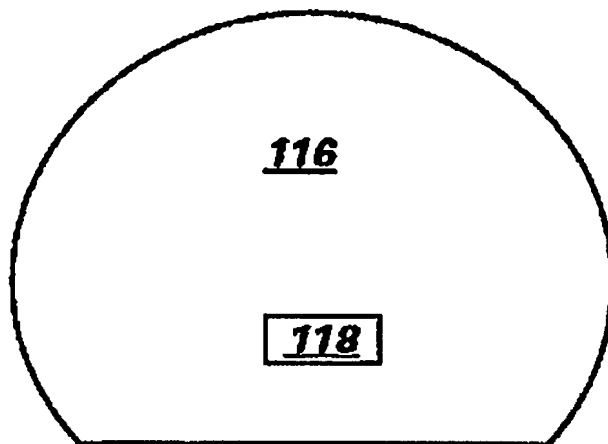


Fig. 15

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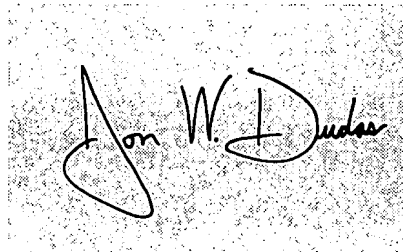
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims:

CLAIM 2, COLUMN 8, LINE 29, change "comprising;" to --comprising:--

Signed and Sealed this

Thirteenth Day of November, 2007

A handwritten signature in black ink, reading "Jon W. Dudas", is written over a rectangular area with a light gray, textured background.

JON W. DUDAS

Director of the United States Patent and Trademark Office

(12) **United States Patent**
Farnworth

(10) Patent No.: **US 7,170,361 B1**
(45) Date of Patent: **Jan. 30, 2007**

(54) **METHOD AND APPARATUS OF
INTERPOSING VOLTAGE REFERENCE
TRACES BETWEEN SIGNAL TRACES IN
SEMICONDUCTOR DEVICES**

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(US)**

(73) Assignee: **Micron Technology, Inc., Boise, ID
(US)**

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/548,942

(22) Filed: Apr. 13, 2000

(51) Int. Cl. **H01P 3/08** (2006.01)

(52) U.S. Cl. 333/1; 333/238; 333/247;
257/778; 257/780

(58) Field of Classification Search 333/1,
333/238, 246, 247; 257/778, 780
See application file for complete search history.

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* cited by examiner

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(74) Attorney, Agent, or Firm—TraskBritt

(57) **ABSTRACT**

A method and apparatus for substantially reducing or eliminating electromagnetic and electrostatic coupling between signal traces on a substrate is disclosed. A substrate, such as a printed circuit board, is formed with an electrically insulative layer and a conductive layer. A portion of the conductive layer is removed to form circuit traces including signal traces and voltage reference traces configured such that each signal trace is separated from each other signal trace by at least one voltage reference trace. The invention is also applied to multiple layer printed circuit boards including a single voltage reference plane, an electronic system, and a semiconductor substrate. According to another aspect of the invention, a majority of a conductive layer is left on an insulative layer of a substrate by removing only those portions of the conductive layer immediately adjacent signal traces such that the remaining conductive material, which is ordinarily removed, acts to couple electromagnetic and electrostatic fields from the signal traces.

3 Claims, 4 Drawing Sheets

